REMARKS

Claims 1-15 are all of the claims presently pending in the present Application. Claims 1-7 have been amended to more particularly define the invention. Claims 8-15 have been added to claim additional features of the invention.

It is noted that the claim amendments herein are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims, or for any statutory requirements of patentability.

Further, it is noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Applicant gratefully acknowledges the Examiner's indication that claims 4 and 7 would be allowable if rewritten in independent form. However, Applicant respectfully submits that all of the claims are allowable.

Claims 1-3 and 5-6 stand rejected under 35 U.S.C. § 102(e) as being allegedly anticipated by Coughlin, Jr. et al. (U. S. Patent Pub. No. 2003/0146774).

This rejection is respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (e.g., as recited in claim 1) is directed to an output buffer apparatus which includes first and second power supply terminals, an output terminal, a main-buffer circuit including a plurality of first transistors which are connected between said first power supply terminal and said output terminal and a plurality of second transistors which are connected between said second power supply terminal and said output terminal, and a pre-buffer circuit including a plurality of first pre-drivers one of said first pre-drivers driving one of said first transistors in accordance with a data signal and a plurality of second pre-drivers one of said second pre-drivers driving one of said second transistors in accordance with said data signal.

Importantly, the apparatus also includes a plurality of first sequential circuits which receive a first impedance adjusting signal in synchronization with said data signal to turn ON one of said first pre-drivers, and a plurality of second sequential circuits which receive a second impedance adjusting signal in synchronization with said data signal to turn ON one of said second pre-drivers.

In a conventional output buffer apparatus, a calibrating operation is always carried out so that the output signal at the output terminal may be changed in the middle of data "1" or "0". That is the output signal at the output terminal is distorted, thus deteriorating the quality of the output signal at the output terminal (Application at page 11, line 26-page 12, line 2.

The claimed invention, on the other hand, includes a plurality of first sequential circuits which receive a first impedance adjusting signal in synchronization with said data signal to turn ON one of said first pre-drivers, and a plurality of second sequential circuits which receive a second impedance adjusting signal in synchronization with said data signal to turn ON one of said second pre-drivers (Application at page 11, line 25-page 12, line 12; Figure 10). In the claimed invention, since the calibrating operation is carried out (e.g., always carried out), the impedance codes RUP and RDN may be renewed and fetched by the pre-buffer circuit 1 in synchronization with the date reading operation of the pre-buffer circuit and the main-buffer circuit 2, so that the output signal at the output terminal may not be changed in the middle of a data "1" or "0". That is the output signal a the output terminal is not distorted (Application at page 12, lines 24-33).

II. COUGHLIN, JR.

The Examiner alleges that Coughlin, Jr. teaches the claimed invention of claims 1-3 and 5-6. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Coughlin, Jr.

Coughlin, Jr. discloses an impedance control circuit which includes a controlled

input/output cell 16 having a P/N-bit control interface and driver impedance update logic (Coughlin, Jr. at [0025]). The logic (e.g., see Figure 4 in Coughlin, Jr.) includes internal latches 22 that hold input control bits. pFET control bits are passed to the driver pull-up during a "one" to "zero" transition, and nFET control bits are passed to the driver pull-down during a "zero" to "one" transition.

However, Coughlin, Jr. does not teach or suggest "*a plurality of first sequential circuits which receive a first impedance adjusting signal in synchronization with said data signal to turn ON one of said first pre-drivers; and a plurality of second sequential circuits which receive a second impedance adjusting signal in synchronization with said data signal to turn ON one of said second pre-drivers*", as recited, for example, in claim 1.

As noted above, in the claimed invention, since the calibrating operation is carried out (e.g., always carried out), the impedance codes RUP and RDN may be renewed and fetched by the pre-buffer circuit 1 in synchronization with the date reading operation of the pre-buffer circuit and the main-buffer circuit 2, so that the output signal at the output terminal may not be changed in the middle of a data "1" or "0". That is, the output signal at the output terminal is not distorted (Application at page 12, lines 24-33).

Clearly, this is not taught or suggested by Coughlin, Jr. Indeed, the Examiner attempts to equate the internal latches 22 in Coughlin, Jr. with the plurality of first sequential circuits and plurality of second sequential circuits of the claimed invention. However, this is clearly incorrect.

In fact, Coughlin, Jr. merely teaches that the internal latches 22 receive pFET control bits (PVTP) and hold the input control bits. Coughlin, Jr. merely states that the pFET control bits are passed to the driver pull-up during a "one" to "zero" transition (Coughlin at [0025]). That is, **nowhere does Coughlin, Jr. teach or suggest that the internal latches 22 receive a first impedance adjusting signal in synchronization with a data signal to turn ON one of the first pre-drivers**.

Therefore, Applicant submits that Coughlin, Jr. does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

Applicant notes that Replacement sheets for Figure 6, Figure 14A and Figure 15A are submitted concurrently herewith. Figure 6 has been corrected to replace "CALIBRATING OPERATION IMPEDANCE CODES RUO & RDN" with "CALIBRATING OPERATION IMPEDANCE CODES RUP & RDN". Figure 14A has been corrected to correctly identify the clock signals C1 and C1 at transfer gate 1407. Figure 15A has been corrected to replace "1i' - 1 (i = 1, 2,..., n)" with "1i' - 2 (i = 1, 2,..., n)" and to correctly identify the clock signals C2 and C2 at transfer gate 1417.

In view of the foregoing, Applicant submits that claims 1-15, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 5/21/05

Phillip E. Miller
Reg. No. 46,060

McGinn & Gibb, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254